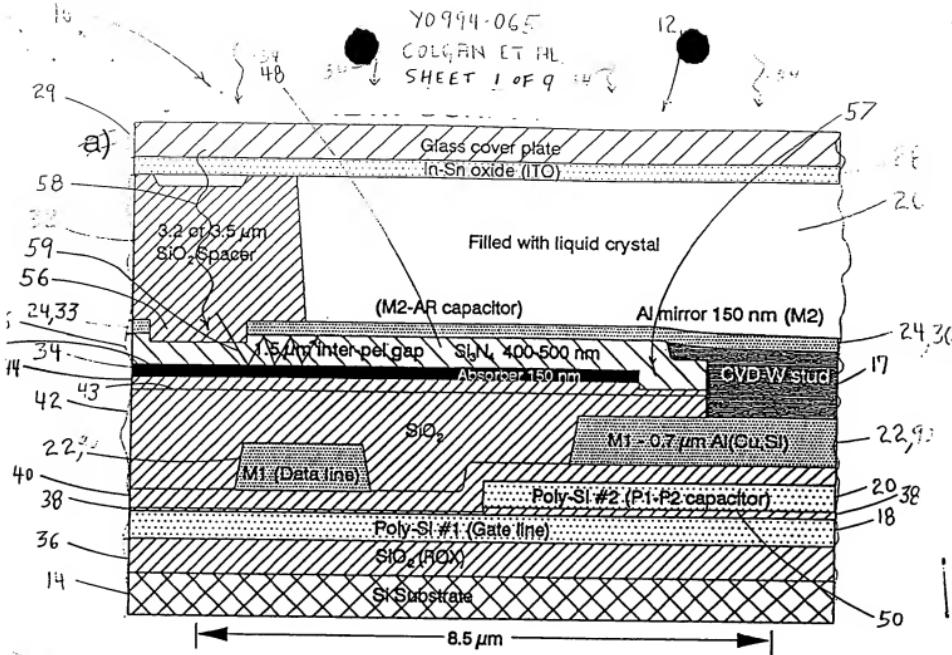


ORIGINALLY SUBMITTED INFORMAL DRAWINGS

YO994-065XX

Serial No. 08/999,663



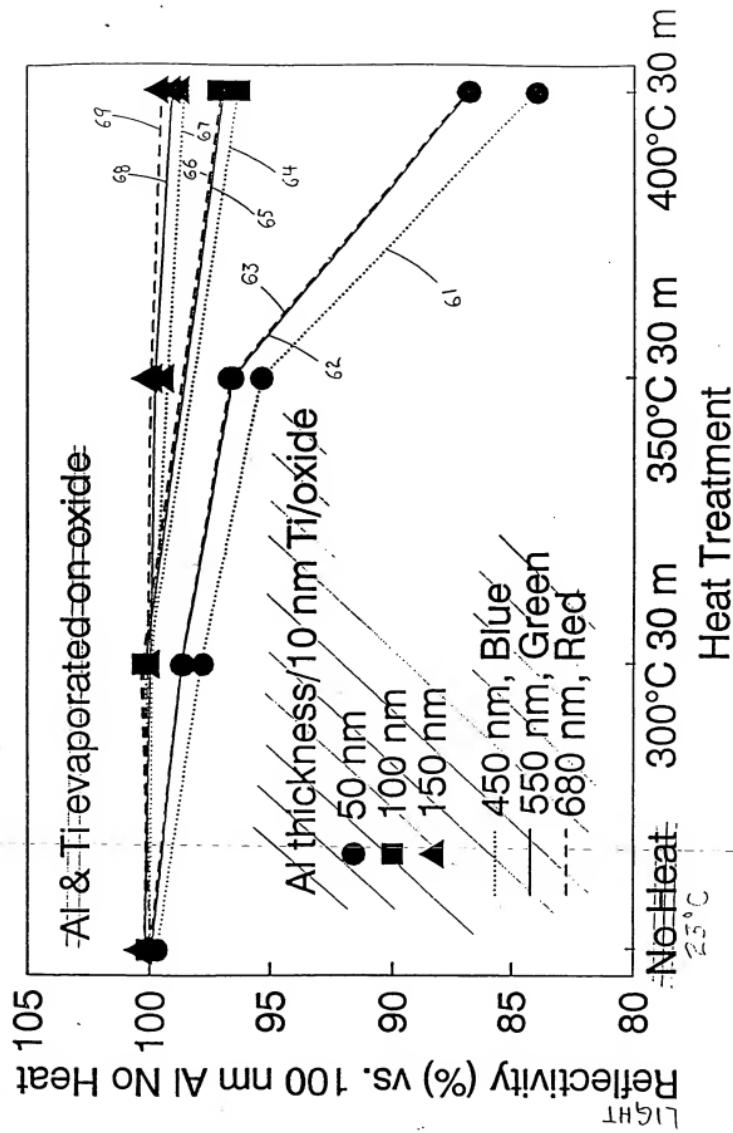


Fig. 2

ARC2

Annealing (1 h at each temperature)

200°C 350°C + 200°C 400°C + 200°C

-Bulk Al reflectivity \approx 92%
-Al(Cu) has less hillocks with annealing

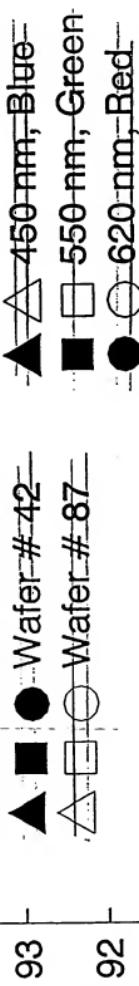
LIGHT ABSOLUTE
REFLECTIVITY (Percent)

92 90 88 86

177 nm Al
 177 nm Al

94

-After-M2-(Mirror)=patterning-



DGLHT Reflectivity (absolute %)

68

C1 (M2 no topography) OP2

Test Structure

OD3

Fig. 4

AACK

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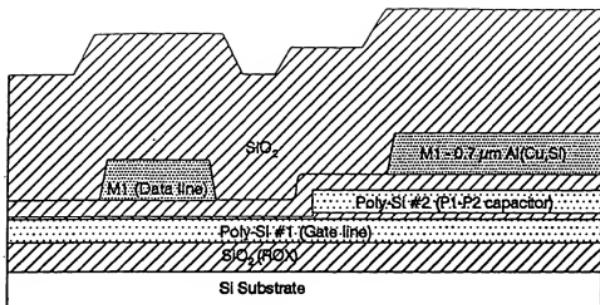


FIG 5

a) Lift off 0.7 μm Al(Cu, Si) M1.
Deposit thick oxide.

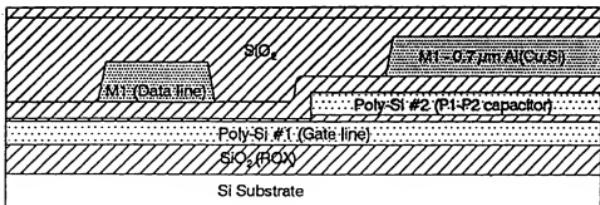


FIG 6

b) CMP oxide leaving 500 nm
on highest M1 point.
Deposit 200 nm oxide.

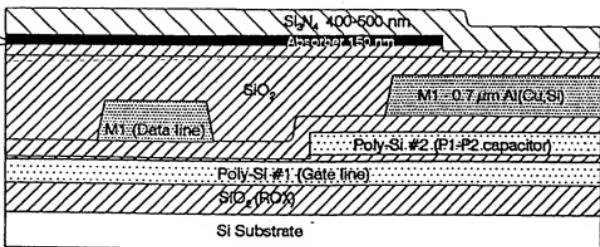


FIG 7

c) Deposit 10 nm Ti/ 100 nm
Al/ 50 nm TiN, pattern with
AR mask.
Deposit 400-500 nm nitride.

~~Fig. 5(a-c)~~

IB M Confidential

ARC6A

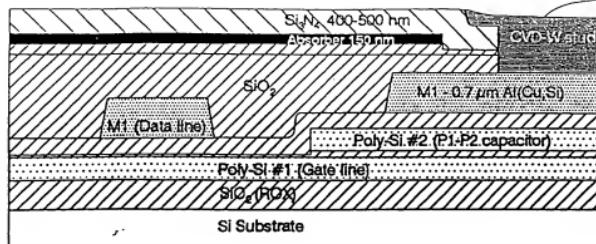


FIG 8

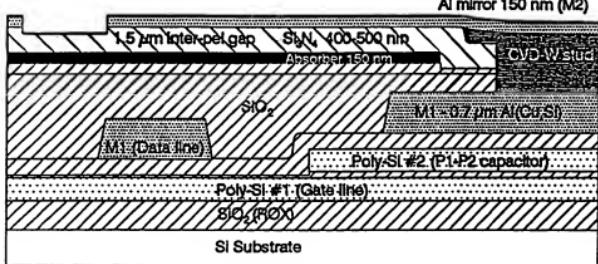


FIG 9

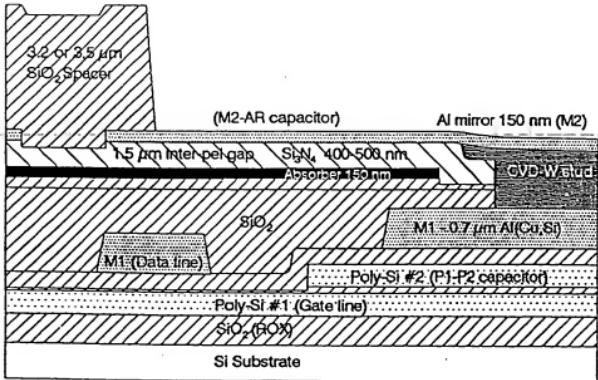


Fig. 5(d-f)

FIG 10

APPROVED: /JD/
08/06/2008

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a) $15 \mu\text{m}$

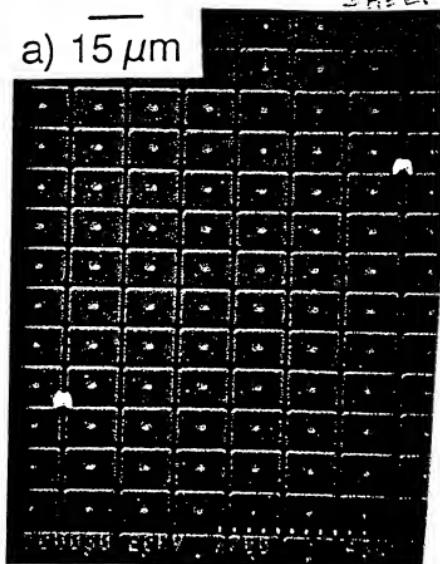


Fig. 11

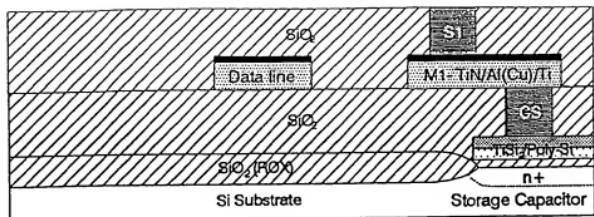


Fig. 12

a) Use standard CMOS 4 process to Si1.

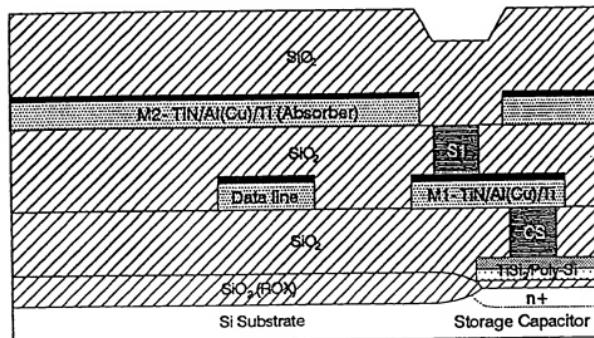
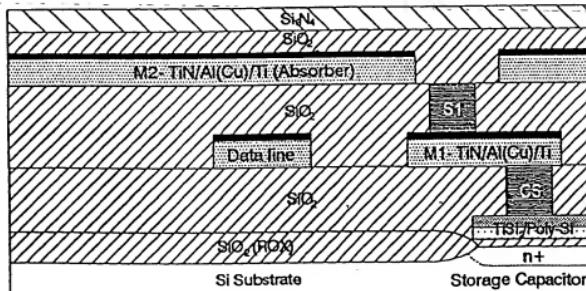


Fig. 13

b) Pattern POR M2 as Absorber layer. POR oxide deposition.



c) CMP-oxide leaving 500 nm on highest M2 point.
Deposit 300 nm nitride.

Fig. 8(a-c)

Fig. 14

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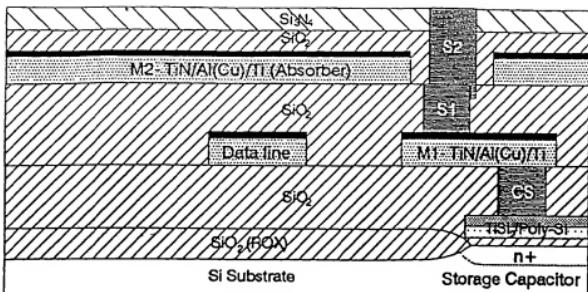


FIG 15
M3- 150 nm Al or Al(Cu)/10 nm Ti (Mirror)

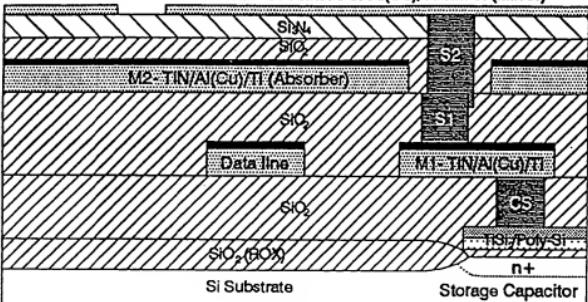


FIG 16

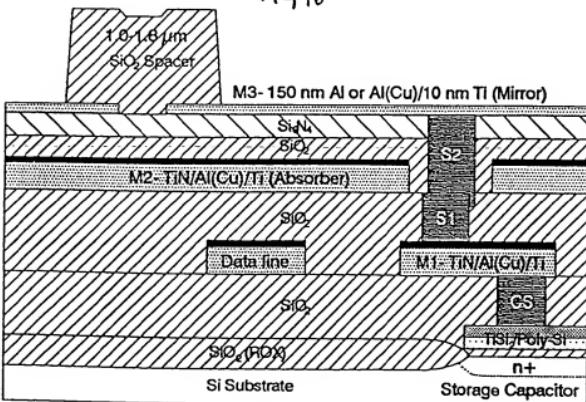


Fig. 8(d-f)

FIG 17

d) Pattern with S2 mask.
Deposit liner & CVD-W.
W Chem-mech polish.
Stacked S1&S2 to
connect M1 & M3.

e) Deposit 10 nm Ti/ 150 nm
Al, pattern with M3 mask.

f) Deposit 1.0 or 1.8 μ m oxide,
pattern with SP mask. Open
up M2 pads with TV mask.